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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/714,893	11/18/2003	Yasuhiro Iwashita	1248-0680P	2811
2292 7590 02/21/2007 BIRCH STEWART KOLASCH & BIRCH PO BOX 747 FALLS CHURCH, VA 22040-0747			EXAMINER CAVALLARI, DANIEL J	
			ART UNIT	PAPER NUMBER
			2836	
SHORTENED STATUTORY PERIOD OF RESPONSE		NOTIFICATION DATE	DELIVERY MODE	
3 MONTHS		02/21/2007	ELECTRONIC	

**Please find below and/or attached an Office communication concerning this application or proceeding.**

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

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mailroom@bskb.com

<b>Office Action Summary</b>	Application No. 10/714,893	Applicant(s) IWASHITA, YASUHIRO	
	Examiner Daniel J. Cavallari	Art Unit 2836	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

#### Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

#### Status

- 1) ☒ Responsive to communication(s) filed on 22 November 2006.
- 2a) ☒ This action is FINAL.                      2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

#### Disposition of Claims

- 4) ☒ Claim(s) 1,2 and 4-13 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1,2 and 4-11 is/are rejected.
- 7) ☒ Claim(s) 12,13 is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

#### Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

#### Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All    b) ☐ Some \*    c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
  2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

#### Attachment(s)

- |  |   |
|--|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892)                     | 4) <input type="checkbox"/> Interview Summary (PTO-413)           |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____                                      |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08)          | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| Paper No(s)/Mail Date _____  | 6) <input type="checkbox"/> Other: _____                          |

### **DETAILED ACTION**

The examiner acknowledges a submission of the amendment filed on 11/22/2006. The amendments to the abstract and claims 1, 2, 4, 6, 9, 10, & 11 and cancellation of claim 3 are accepted.

### ***Response to Arguments***

Applicant's arguments, see pages 5-7, filed 11/22/2006, with respect to the objection to claim 1 and 112 first paragraph rejection of claim 6 have been fully considered and are persuasive. The previously made objection and rejection of these claims have been withdrawn.

The previously made 112 second paragraph rejection of claim 2 has been withdrawn in view of the amendments.

Applicant's arguments with respect to the 103 rejections of claims 1-11, filed 11/22/2006, have been fully considered but they are not persuasive.

The applicant argues that Blair fails to teach "A specified voltage sensor section for detecting an output from a specified one of the secondary circuits..." The examiner notes that Blair teaches a sensing circuit (32) for sensing the "a specified one" (Vout2) of the secondary circuit and notes that although the circuit also senses another voltage, the claims do not limit to just one voltage.

In response to applicant's argument that the references fail to show certain features of applicant's invention, it is noted that the features upon which applicant relies (i.e., "the total power sensor section detects the total secondary power") are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

The examiner notes that the claim reads "...a total power sensor section for detecting a value in accordance with a total secondary power which is a sum of power outputs to all secondary circuits" and does not limit the total power sensor to detecting the total secondary power as the applicant suggested in the arguments but rather only for a "total power sensor section" for "detecting a values in accordance with a total secondary power which is a sum of power outputs to all the secondary circuits". The examiner notes that the "value" ( $V_{out1}$ - $V_{outN}$ ) is "in accordance" with the total secondary power which is a sum of power outputs to all secondary circuits as the "value"  $V_{out1}$  to  $V_{outN}$  plus  $V_{out1}$  multiplied by their respective output currents would equal the total secondary power as provided by ohms law.

### ***Claim Rejections - 35 USC § 103***

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 1, 2, & 4-9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Blair (US 6,211,579) in view of Rozman (US 5,541,828) and in further view of Melse (US 5,933,049).

In regard to Claim 1, 5, 6, & 9

Blair teaches:

- A DC-DC converter (12) with multiple voltage outputs (Vout1- VoutN) (See Figure 1).
- A specified voltage sensor (32) for detecting output voltage from a specified one (Vout2) of the secondary circuits.
- An output limiting section (30) for limiting an electric power output [the power output to Vout1] to at least one non-specified secondary circuit (Vout1) when the specified-voltage sensor (32) section has detected a voltage being equal to a first predefined value in the specified secondary circuit (Vout2) [Read on by the sensor sensing a voltage drop in the output and controlling the impedance source (30) thereby limiting the output power] (See Column 2, Lines 51-67).
- The output limiting section including a total power sensor section (control circuit of converter 12) (See Column 2, Lines 56-60) for detecting a value (voltages Vout2-VoutN) in accordance with a total secondary power (See Column 2, Lines 43-67) [The examiner notes that the signal detected on line 22 is disclosed as being controlled by the sensing circuit (32) which is "in accordance" with a total secondary power (Vout2-VoutN) of all the secondary circuits as it controls the

sensing circuit which controls the adjustable impedance (30) which in turn is detected by the converter "control circuit" (not shown) and controls the "pulse width modulator" (not shown) of the DC-DC converter (12) (See Figure 12 & Column 2, Lines 56-60).

Blair fails to explicitly teach the details of the DC-DC converter, remaining silent in regards to the use of a transformer however states that the converter "may comprise, for example, the converter which is described and illustrated in U.S. Patent No. 5, 541, 828" (See Column 2, Lines 27-31).

Blair teaches a DC-DC converter comprising a primary circuit [read on by the circuit on the primary side of the transformer of Figure 5] which includes a primary winding (np) and a switching device (Q1) (See Figure 5) and a plurality of secondary circuits each including a secondary winding wherein the switching device turning on/off power to the primary winding to produce secondary electric power applied from the secondary windings to the loads (See Figure 5 & Column 2, Lines 50-64 & Column 4, Lines 6-13).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the DC-DC converter taught by Rozman into the regulation circuit taught by Blair as suggested by Blair (See Column 2, Lines 27-39). The motivation would have been to provide a converter that is known in the art and in which to supply multiple outputs to the multiple loads taught by Blair and which efficiently utilizes its power transformer (See Rozman Column 1, line 65 to Column 2, Line 11).

Blair fails to teach quasi-short circuiting the output lines of the specified and non-specified secondary side when the specified voltage sensor section has detected the voltage being more than or equal to a first predefined value.

Melse teaches a power supply circuit in which a short circuit switch (10) is used between the secondary winding of a transformer and a load (8) and positioned in series between the output lines of a secondary circuit and controlled in response to a reference voltage in which to control the output to operate at a certain value for powering the load device (See Column 5, Lines 29-38).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the short circuit device (10) into the specified and non-specified secondary side circuits of Blair in which the sensor controls the switch in response to a specified voltage being equal to a first predefined value as taught by Melse [The examiner notes the switch is a "quasi-shorting" device as a switch has an inherent resistance value associated with it]. The motivation would have been to provide greater control of the output voltage to sensitive loads.

Blair further teaches:

In regard to Claim 2

- The specified secondary circuit (Vout2) having a higher voltage than the non-specified secondary circuit (Vout1) (See Column 2, Lines 15-27) in which Blair

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discloses Vout1 as the "low voltage output" and Vout2 as the "high voltage output".

In regard to Claim 7

- A non-specified output voltage sensor (read on by the converter "control circuit") for detecting an output voltage from the at least one non-specified secondary circuit (Vout1) and a control section (read on by the "pulse width modulator") of the DC-DC converter (12) controls turning on/off the switching device based on a detection result from the non-specified output voltage sensor section (See Figure 12 & Column 2, Lines 56-60).

In regard to Claim 8

- The specified secondary circuit (Vout2) including an output voltage regulator (20) between the specified voltage sensor (32) and load (LOADN) (See Figure 1 & Column 2, Lines 15-27).

In regard to Claim 4

Blair teaches the output limiting section including a total power sensor section ("control circuit" of converter 12) (See Column 2, Lines 56-60) for detecting a value in accordance with a total secondary power but fails to explicitly teach whether this circuit senses voltage or current.



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Melse explicitly teaches a sensor (9) capable of sensing both current and voltage and comparing it with either a reference current or voltage in order to control a switch (See Column 5, Lines 29-38). It would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the current sensor taught by Melse. The motivation would have been to adequately sense the feedback via current by means well known in the art in which to control the circuit.

Claim 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over Blair, Rozman, Melse and in further view of Ohsawa et al. (US 4,236,198)

Incorporating all arguments above of the power supply system taught by Blair, Blair fails to teach the control section including a latch function which stops driving the switch when the total power is more than or equal to a predefined value.

Ohsawa et al. (hereinafter referred to as Ohsawa) teaches a switching regulator which has a control section with a latch function (read on by holding circuit 21) which stops the driving of the switch device (7) when the detection circuit (17) indicates the total secondary power is more than or equals to a second predefined value (read on by the over current detection on the primary side which is representative of the total power on the secondary side) and which reverts to a previous condition when an electric power is restored (read on by the resetting of the over current detector by the reset circuit 22) (See Figure 3 & Column 4, Line 32 to Column 5, Line 3).

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Claim 11 is rejected under 35 U.S.C. 103(a) as being unpatentable over Blair & Rozman, Melse and in further view of Tai (US 5,450,308).

Incorporating all arguments above of the power supply system taught by Blair and Melse, Blair and Melse teach a power supply device in which an electronic switch is used in a short circuit section however fails to explicitly teach the switch being a thyristor.

Tai teaches a short circuit device (1) comprising a thyristor (GTO) (See Figure 1 & Column 3, Lines 37-57).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the thyristor taught by Tai in to the short circuit device of Blair and Melse as it is commonly known in the art to use a thyristor in place of a controllable switch as they are inexpensive, easy to operate, and easily available.

#### ***Allowable Subject Matter***

Claims 12 & 13 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Prior art fails to teach applying a holding current through a thyristor to produce the quasi-short circuit through the thyristor even when the load of the specified secondary circuit is shorted out.

***Conclusion***

**THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Daniel J. Cavallari whose telephone number is (571)272-8541. The examiner can normally be reached on Monday-Friday 8:30-5:00.

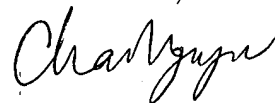
If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Brian Sircus can be reached on (571)272-2800 x36. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

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Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Daniel Cavallari

February 5, 2007



**CHAU N. NGUYEN**  
**PRIMARY EXAMINER**